

PTO/SB/08A (Substitute for form 1449/PTO)	Attorney Docket No.: 026-0044
	Application No.: 10/813,837
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Akhil K. Garlapati
	Filing Date: March 31, 2004
	Group Art Unit: 2838
	Examiner Name: Patel, Rajnikant B.
Sheet 1 of 1	Date Submitted: January 30, 2006

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ² -Number ⁴ -Kind Code ³ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
Examiner Signature			Date Considered	3/11/06		

***EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1. Applicant's unique citation designation number (optional).

²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04.

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⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.

⁶Applicant is to place a check mark here if English language Translation is attached.

U.S. Department of Commerce, Patent and Trademark Office		Attorney Docket No.: 026-0044				
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant(s): Garlapati et al.				
(Use several sheets if necessary)		Filing Date: March 31, 2004				
JUL 16 2004 P A T E N T & T R A D E M A R K S O U R C E		Group Art Unit: 2819				
		Date Submitted: July 14, 2004				
U.S. Patent Documents						
*Examiner Initial		Document Number	Date	Name		
<i>C</i>	AA	4,588,941	May 13, 1986	Kerth et al.		
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<i>C</i>	AL	JP 1292411 (English abstract)	Nov. 24, 1989	Japan		
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<i>C</i>	AM	Allen et al., "Current and Voltage References," <u>CMOS Analog Circuit Design</u> , 1987, pp. 240-252.				
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<i>A</i>	AO	Banba et al., "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," IEEE Journal of Solid-State Circuits, Vol. 34, No. 5, May, 1999, pp. 670-674.				
Examiner <i>Ref. Lai</i>		Date Considered	3/1/06			
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<i>J</i>	AP	6,052,020	Apr. 18, 2000	Doyle
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					Translation	
		Document	Date	Country	Yes	No

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<i>K</i>	AT	de Langen et al., "Compact Low-voltage PTAT-Current Source and Bandgap-Reference Circuits," Delft Institute for MicroElectronics and Submicron technology (DIMES), pp. 108-111.
<i>R</i>	AU	Gray et al., "Band-Gap-Referenced Biasing Circuits," <u>Analysis and Design of Analog Integrated Circuits</u> , Third Edition, 1993, pp. 338-346.
<i>R</i>	AV	Lee, "Bandgap References in CMOS Technology," <u>The Design of CMOS Radio-Frequency Integrated Circuits</u> , 1998, pp. 233-235.
<i>R</i>	AW	Razavi, "Bandgap Reference," <u>Design of Analog CMOS Integrated Circuits</u> , 2001, pp. 384-392.
<i>R</i>	AX	Phang et al., "Low Voltage, Low Power CMOS Bandgap References," ECE 1352, University of Toronto, pp. 1-17.

Examiner	<i>By - [Signature]</i>	Date Considered	3/11/06
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